AMENDMENTS TO THE CLAIMS

Claims 1-19. (Cancelled)

20. (Original) A method of providing custom design files for programmable logic devices (PLDs), the PLDs each having a unique identifier, the method comprising:

testing a plurality of the PLDs and selecting therefrom a plurality of defective PLDs containing localized defects;

recording defect data for each defective PLD, the defect data comprising the unique identifier for each defective PLD and location information for each detected defect within the defective PLD;

maintaining a database of the defect data;

receiving a first design file from a user, the design file being an implementation targeted towards a fully functional version of the defective PLDs;

receiving a first identifier from the user uniquely identifying a first defective PLD of the plurality of defective PLDs;

retrieving from the database, based on the first identifier, first location information for the first defective PLD;

performing an incremental compilation with respect to the first design file while using the first location information to avoid the localized defects of the first defective PLD, the incremental compilation generating a second design file; and

providing the second design file to the user.

21. (Original) The method of Claim 20, wherein:

receiving the first identifier from the user is accomplished via a data communications link; and

providing the second design file to the user is accomplished via the data communications link.

22. (Original) The method of Claim 20, further comprising:

receiving a second identifier from the user uniquely identifying a second defective PLD of the plurality of defective PLDs;

retrieving from the database, based on the second identifier, second location information for the second defective PLD;

performing a second incremental compilation with respect to the first design file while using the second location information to avoid the localized defects of the second defective PLD, the second incremental compilation generating a third design file; and

providing the third design file to the user.

23. (Original) The method of Claim 20, wherein the PLD is a field programmable gate array (FPGA).

24. (Original) The method of Claim 23, wherein maintaining the database of the defect data comprises:

generating a defect map for each defective PLD; and

generating a constraints file for each defective PLD based on a corresponding defect map,

and wherein performing an incremental compilation with respect to the first design file comprises using the constraints file corresponding to the first defective PLD.

Claims 25-39. (Cancelled)

40. (New) A method of providing design files for programmable logic devices (PLDs), the method comprising:

establishing a database of defect data for a plurality of defective PLDs, the defect data including a unique identifier for each defective PLD in association with location information for each defect within the defective PLD;

receiving a first design file from a user, the design file being an implementation targeted to a non-defective PLD;

receiving from the user a first identifier that uniquely identifies a first defective PLD of the plurality of defective PLDs;

retrieving from the database, based on the first identifier, first location information for the first defective PLD;

performing an incremental compilation of the first design file while using the first location information to avoid each defect of the first defective PLD, the incremental compilation generating a second design file; and

providing the second design file to the user.

41. (New) The method of claim 40, further comprising:

receiving from the user a second identifier that uniquely identifies a second defective PLD of the plurality of defective PLDs;

retrieving from the database, based on the second identifier, second location information for the second defective PLD;

performing a second incremental compilation of the first design file while using the second location information to avoid each defect of the second defective PLD, the second incremental compilation generating a third design file; and

providing the third design file to the user.

42. (New) The method of claim 40, wherein the PLD is a field programmable gate array (FPGA).

43. (New) The method of Claim 42, wherein maintaining the database of the defect data comprises:

generating a defect map for each defective PLD; and

generating a constraints file for each defective PLD based on a corresponding defect map,

and wherein performing an incremental compilation of the first design file comprises using the constraints file corresponding to the first defective PLD.